C-3

OPTIMUM DESIGN OF NON LINEAR POWER FET AMPLIFIERS

C. GUO*, M. CAMIADE**, D. ROUSSET*, A. CESSEY**, J. OBREGON*, A. BERT**

* IRCOM Université de Limoges - CNRS 87060 LIMOGES Cédex - FRANCE
** THOMSON Composants DHM, 29 Avenue Carnot, 91302 MASSY - FRANCE

ABSTRACT

In this paper, an efficient approach to optimum design of power amplifiers stages is described. The impedances presented to the FET are optimized independently of the topology chosen for their realization. They are then synthetized by usual methods of linear circuits.

The proposed method has been applied to the design of broadband power FET amplifiers. The realizations have given a good correlation between the theoretical and experimental results. Moreover, the method may be used to the optimum design of power FET multipliers.

I - INTRODUCTION

Optimization of non-linear circuits is a formidable task for microwave engineering in the next years to come.

A non linear circuit may be defined by at least one semi-conductor device and a linear embedding circuit. Usual method of optimization of these circuits is generally done by first fixing "a priori" a topology, and then optimizing the values of the linear elements afterwards. But is the topology chosen the best one ? In fact, this design method of non-linear circuits is directly derived of that used of the linear ones.

In this paper, a new approach to the optimization of non-linear circuits is proposed. It allows to find the upper limits that can be achieved with a given active device. It has been successfully tested on power FET amplifier design.

II - PROPOSED OPTIMIZATION METHOD

Given a field effect transistor defined by a time dependent non-linear model, let us suppose that we want to optimize the added-power of the device, to use it in a one stage power-amplifier.

In mathematical form, the device model describes the functional relationships between dependent and independent port variables. For the FET under analysis these relations may be written in a general form valid for all non-linear two port circuits as :

$$i_1(t) = F_{NL}(v_1(t), v_2(t))$$

$$i_2(t) = G_{NL}(v_1(t), v_2(t))$$

However, it is well known that the dependent variables in an FET are in fact functions $v_{gs}(t)$ and $v_{ds}(t)$ (see Fig.1) ; so in this case, $i_1(t)$ and $i_2(t)$ may be defined as functions of $v_{gs}(t)$ and $v_{ds}(t)$. These latter voltages are now the independent variables ; and we may write :

$$i_1(t) = F_{NL}(v_{gs}(t), v_{ds}(t)) \quad (1)$$

$$i_2(t) = G_{NL}(v_{gs}(t), v_{ds}(t)) \quad (2)$$

From these equations it is clear that the behaviour of the device is completely defined by the knowledge of the independent waveforms :

$$v_{gs}(t)=v_{gs0}+v_{gs1}\cos(\omega_o t+\psi_1)+v_{gs2}\cos(2\omega_o t+\psi_2)+\ldots \quad (3)$$

$$v_{ds}(t)=v_{ds0}+v_{ds1}\cos\omega_o t+v_{ds2}\cos(2\omega_o t-\phi_2)+\ldots \quad (4)$$

Introducing equations (3) and (4) in (1) and (2), and by using the discrete Fourier transform, the dependent variables (port-currents) $i_1(t)$ and $i_2(t)$ may be written in form to Fourier series I_1, I_2.

Defining now the maximum added-power of the FET as the desired feature, one may write the function to be optimized as :

$$P_{add}=f_{NL}[v_{gs}(t), v_{ds}(t)]=\frac{1}{2}\,\mathrm{Re}(-\vec{V}_{21}.\vec{I}^{*}_{21} - \vec{V}_{11}.\vec{I}^{*}_{11})$$

A standard optimization routine [1] may be used to maximize P_{add} as a function of V_{gs} and V_{ds}.

Once optimization is achieved, bias voltages and FET-loads are known from $\vec{V}_{gs}\Big|_{opt}$ and $\vec{V}_{ds}\Big|_{opt}$.

Our proposed process leads to a global optimization of the overall non-linear circuit. Indeed :

- on one hand, the values of the access variables of the semi-conductor device have been optimized for the desired objective function,
- on the other hand, the linear embedding network is synthetized to support these optimized variables as input admissible signals at their own ports.

III - NON LINEAR FET MODEL - DETERMINATION OF THE NON LINEARITIES

a) Large signal dynamic GaAs MESFET model

The FET used is the FUJITSU FLR024

Fig.1 shows the equivalent circuit model in which

0149-645X/87/0000-0111$01.00 © 1987 IEEE

four main non-linear elements of GaAs MESFET have been considered. They are :

- the input Schottky diode Ggs representing gate current in the gate-source junction ;
- the gate-source capacitance Cgs ;
- the drain current source I_{ds} ; [2]
- the drain-gate voltage controlled-current source I_{gd} describing the drain-gate avalanche current.

b) Determination of the FET model elements :

- determination of linear elements :

In order to obtain more precise values, the measurements are effected in two steps. DC measurements are used to calculate the values of the resistances Rg, Rs and Rd, while C_{gs0} of the gate junction and the values of other linear elements are determined from S parameter measurements in the 2 to 18 GHz.

- determination of non-linear current sources :

To minimize thermal and trapping effects, a pulsed set-up shown in fig.(2) has been developped.

Absorbers allow the FET to be stable from very low frequencies up to microwaves. Short-pulsed voltages V_1 and V_2 with variable amplitudes, widths, and repetition rates, are applied on the gate G and drain D, respectively.

This set-up allows us to measure independently the different current sources, as functions of the external applied voltages. These currents which are functions of V_1 and V_2 are then transformed to internal current sources depending on V_{gs} and V_{ds}, by taking into account the voltage drops in Rg, Rs and Rd. One obtains :

$I_{ds}=f(V_{gs}.V_{ds})$ field effect current

$I_g=g(V_{gs})$ Schottky current

$I_{gd}=h(V_{gs}.V_{ds})$ Avalanche current

These experimental curves are now fitted to the non-linear current expressions.

IV - OPTIMISATION OF THE AMPLIFIER STAGE

The objective is to design a power amplifier giving the maximum added power between 6 GHz and 18 GHz.

Since the bias voltages must be kept constant, they are optimized at 18 GHz and taken as constant at the other frequencies.

Let $\vec{V}_{1i}$, $\vec{V}_{2i}$, $\vec{I}_{1i}$ and $\vec{I}_{2i}$ be the complex voltages and currents at frequencies if$_o$, (i=1, 2, 3...) ports 1, 2. The problem is to maximize :

$$P_{added}=\frac{1}{2}\,Re(-\vec{V}_{21}.\vec{I}^{*}_{21}-\vec{V}_{11}.\vec{I}^{*}_{11})$$

Under the following constraints : [3]

$$Re\left(\frac{\vec{V}_{1i}}{\vec{I}_{1i}}\right) \begin{cases} > C_i, & i=1 \\ \leqslant C_i, & i=2,3,... \end{cases} \quad \text{at port 1}$$

$$Re\left(\frac{\vec{V}_{2i}}{\vec{I}_{1i}}\right) \leqslant D_i, \quad i=1,2,3,... \quad \text{at port 2}$$

where C_i, D_i(i=1,2,3,...) are constants ($C_i \geqslant 0$, $D_i \geqslant 0$)

In the first procedure of optimization, C_i and D_i (i=1,2,3,...) can be chosen equal to zero. If the optimum impedances at ports 1 and 2 are difficult to realize, C_i and D_i must be changed to the positive constants.

V - AMPLIFIER REALIZATION-EXPERIMENTAL RESULTS

Taking into account the results given by the non-linear optimization, a linear embedding circuit operating between 6 and 18 GHz has been synthetized. Note that the resistance placed in the gate stabilizes the transistor out of the operating bandwidth. Fig.3 shows the circuit of one stage medium power amplifier using a typical .5x800 µm FET. The computed curve and experimental points showing the maximum added power versus frequency are shown in Fig.4. Experimental results include the circuit losses, the correlation is better than 1 dB.

The influence of higher harmonics (second, and so on) is very small since the maximum added-power occurs in the "quasi-linear" region (around of 1 dB gain compression).

CONCLUSION

In this paper, a new approach to the optimization of non-linear amplifiers has been described. The key point of this approach is that no topology of the embedding linear network is to be chosen a priori. Hence the performances of the active devices calculated by this method are the upper limits that can be achieved with the given active device. To validate the proposed method, it has been applied to the design of a broadband amplifier. Practical results have shown very good correlation with the theoretical prediction.

The method may be extented to the optimum design of other components such as power multipliers and converters.

REFERENCES

1 - Powell M.J.D., "Non-linear optimization", Academic Press 1982.

2 - Tajima Y., Miller P., "Design of broad-band power GaAs FET Amplifiers", IEEE MTT 32, N°3, March 1984, pp. 621-627.

3 - Albuquerque M.C., Guo C. and Obregon J., "A new approach to fundamental frequency analysis and optimization of non-linear microwave circuits", 15 th. E.M.C., pp. 515-520.

* This work was partially supported by the "Direction des Recherches et Etudes Techniques" (france).

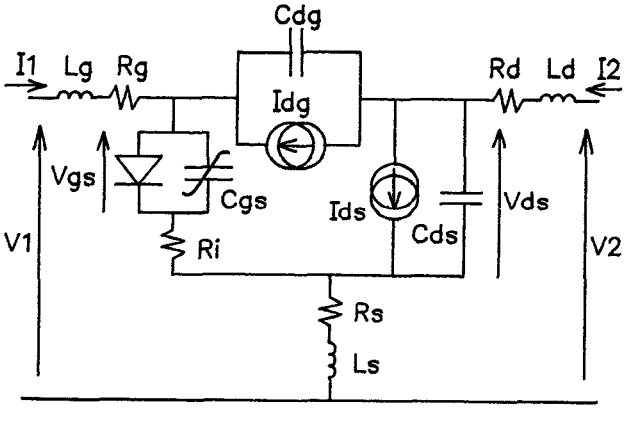

Fig.1. Nonlinear FET model

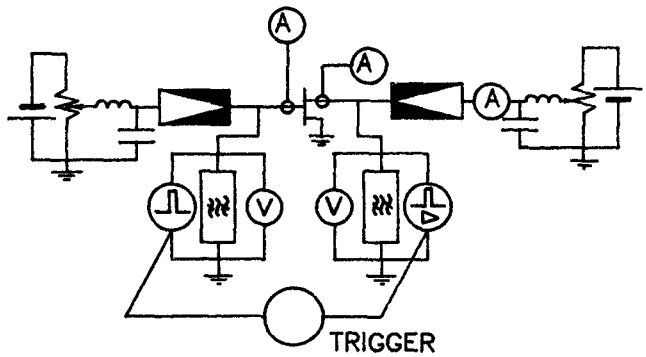

Fig.2. Pulsed measurement set-up

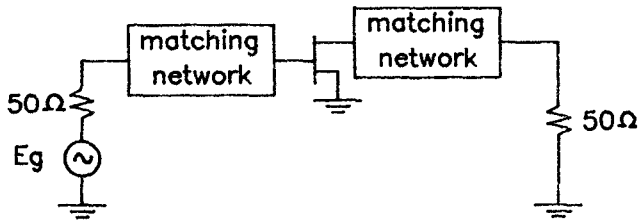

Fig.3. Equivalent circuit of one stage power amplifier

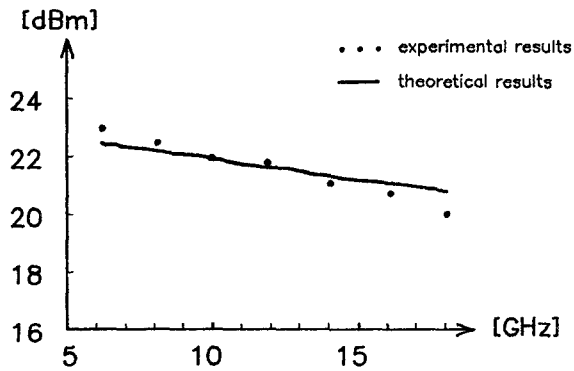

Fig.4. Maximum added power of one stage power amplifier